REMARKS

Claims 1-20 are presently pending in the application. Claims 1-10, 15, 16, and 18 have been amended as to form. Claims 19 and 20 have been added to assure applicant the degree of protection to which his invention entitles him.

The claim amendments are made only to assure grammatical and idiomatic English and improved form under United States practice, and are not made to distinguish the invention over the prior art or narrow the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Method claims 10-18 were rejected under 35 U.S.C. §101, with the contention that they were directed to non-statutory subject matter. Claim 10 has been amended to recite that the claimed method is a computer-implemented method, thereby overcoming this rejection. Claims 19 and 20 have been added to specify use of the fixed point data.

Claims 1-2, 5, 8-11, 14, 17, and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by Ozawa, JP No. 08-101919. Claims 3, 4, 12, and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ozawa. Claims 6, 7, 15, and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ozawa in view of Blackham, et al., U.S. Patent No. 5,619,198. Claims 1, 2, 5, 8-11, 14, 17, and 18 were rejected under 35 U.S.C. §102(b) as being anticipated by Yoshizawa, et al., U.S. Patent No. 5,359,548. Claims 3, 4, 12, and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yoshizawa, et al. Claims 6, 7, 15, and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over

Yoshizawa, et al. and further in view of Blackham, et al. These rejections are respectfully traversed.

THE CLAIMED INVENTION

The claimed invention is directed to a fixed point data generating circuit and method which convert a plurality of floating point data into respective fixed point data. In accordance with exemplary embodiments of the invention, a reference floating point data is determined from the plurality of floating point data. The differences between the value of the exponent part of each of the plurality of inputted floating point data and the value of the exponent part of the reference floating point data are obtained. The mantissa part of each of the floating point data is shifted by the exponent part difference obtained for the corresponding one of the plurality of inputted floating point data, and a predetermined number of bits is extracted from the shifted mantissa part as fixed point data.

THE PRIOR ART REFERENCES

The Ozawa Reference

Ozawa discloses a fixed point data generating circuit which converts a plurality of floating point data into respective fixed point data. A reference floating point data is determined from the plurality of floating point data. The differences between the value of the exponent part of each of the plurality of inputted floating point data and the value of the exponent part of the reference floating point data are obtained. The mantissa part of each of the floating point data is shifted by the exponent part difference obtained for the

corresponding one of the plurality of inputted floating point data. After mantissa shifting, encoding is performed in encoding devices. See Ozawa at the last line of the Abstract.

The Blackham, et al. Reference

Blackham, et al. discloses a number format conversion apparatus in which an input mantissa portion is right shifted, and the resulting "unclipped output mantissa signal" (see Blackham at column 3, lines 14-15) is clipped to a maximum level, if positive, or a minimum level, if negative to produce an output mantissa signal in floating point number format or an output fixed point number signal in fixed point format. See Blackham at column 3, lines 21-26.

The Yoshizawa, et al. Reference

Yoshizawa discloses a fixed point data generating circuit which converts a plurality of floating point data into respective fixed point data. A reference floating point data is determined from the plurality of floating point data. The differences between the value of the exponent part of each of the plurality of inputted floating point data and the value of the exponent part of the reference floating point data are obtained. The mantissa part of each of the floating point data is shifted by the exponent part difference obtained for the corresponding one of the plurality of inputted floating point data. After mantissa sifting, addition and subtraction for the mantissas is executed, in which an adjustment of digit positions is completed. A normalization circuit normalizes and outputs the result of the addition and subtraction. See Yoshizawa at column 11, line 67 to column 12, line 5 and at column 12, lines 41-47.

ARGUMENT

None of the references shows or suggests that a predetermined number of bits be extracted from the shifted mantissa part as fixed point data. Instead, in Ozawa encoding is performed in encoding devices; in Blackman the unclipped output mantissa signal is clipped to a maximum level, if positive, or a minimum level, if negative; in Yoshizawa addition and subtraction for the mantissas is executed, and the result of the addition and subtraction is normalized and outputted.

There is no showing or suggestion of a fixed point data generating circuit in which, once the mantissa is shifted, a predetermined number of bits is extracted from the shifted mantissa part as fixed point data. Accordingly, the claims distinguish patentably from the references and are allowable.

In claims 6 and 15, when an overflow occurs in the bits extracted, the bits extracted are caused to represent the maximum value. In claims 7 and 16 when an overflow occurs by shifting the mantissa part of each of the floating point data, shifted bits are caused to represent the maximum value. In rejecting these claims, the Office Action contends that Blackham shows this. This contention is traversed.

In Blackman, the unclipped output mantissa signal is clipped to a maximum level, if positive, or to a minimum level, if negative to produce an output mantissa signal in floating point number format or an output fixed point number signal in fixed point format. Thus, it is the clipped mantissa signal which is the output signal. There is no showing or suggestion of the bits extracted or the shifted bits representing the maximum signal. Claims 6, 7, 15, and

16 are allowable for this further reason.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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